

A NEW INTEGRATED CIRCUIT FOR CURRENT MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s this scheme was not publicly reported until 1977⁽¹⁾ and has seen rapid development by many authors to date.⁽²⁻⁶⁾ In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e , is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e , instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

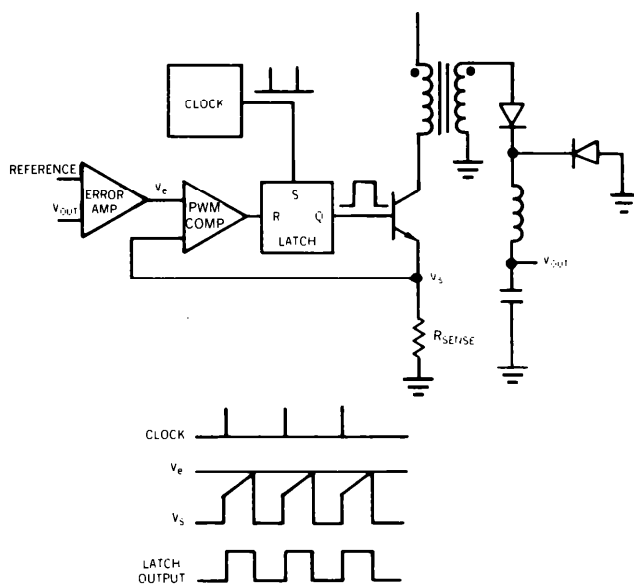


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

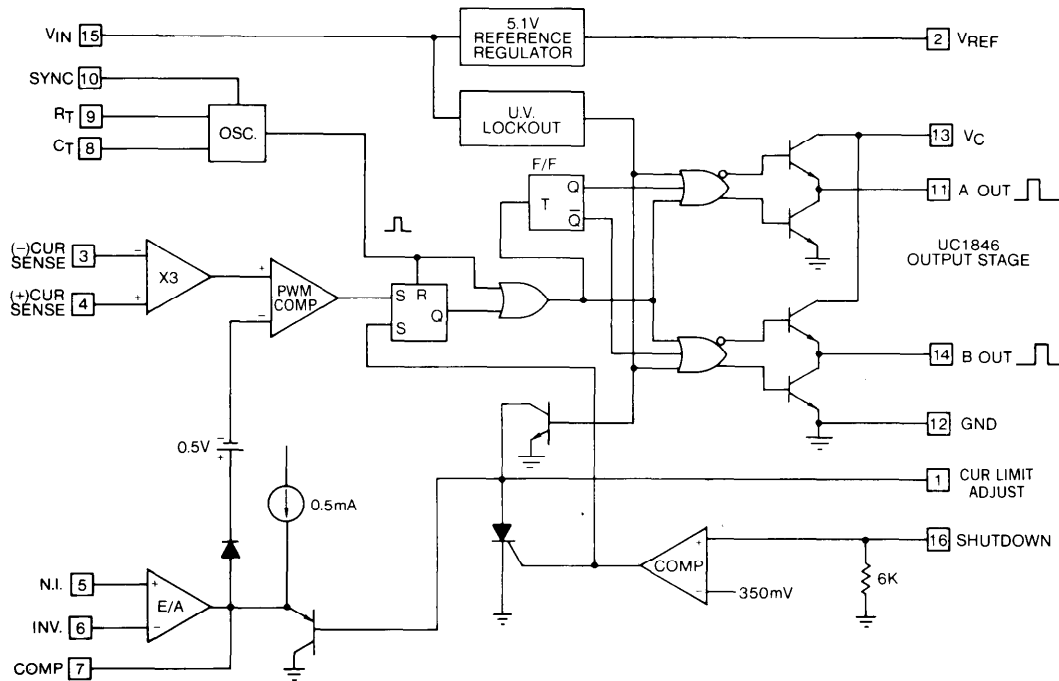


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A $\pm 1\%$, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1 MHz.
- An error amplifier with common mode range from ground to $V_{CC}-2V$.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

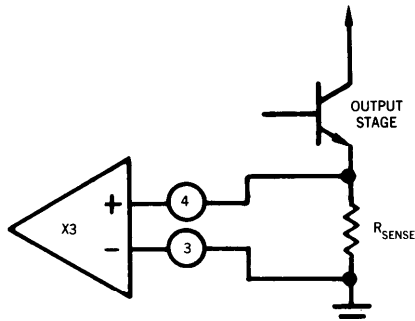
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

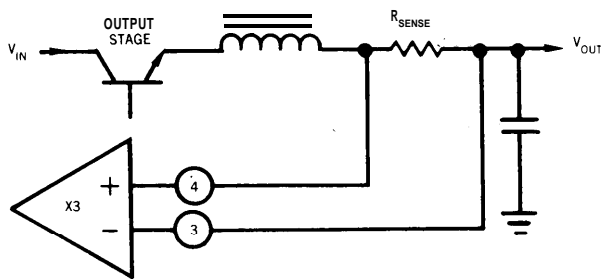
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND

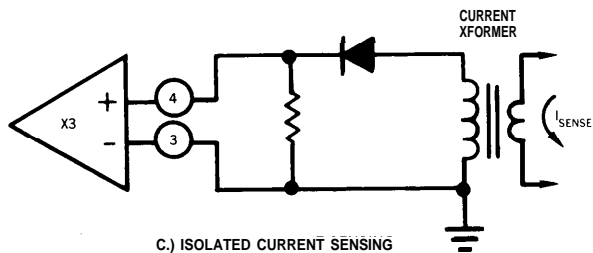


FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in

series with the input is generally all that is required to reduce the spike to an acceptable level.

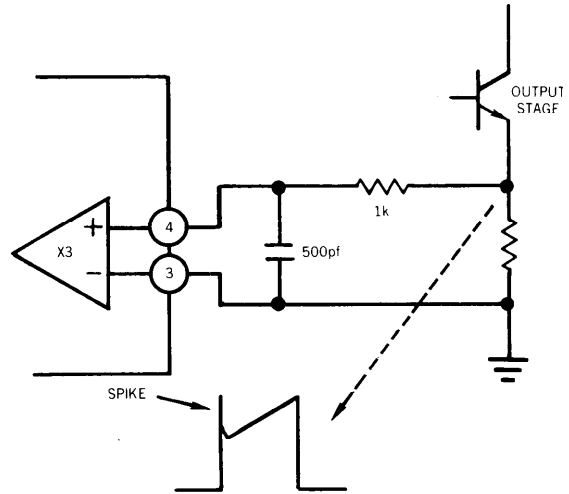


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow ($f_t = 2\text{MHz}$) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1MHz.

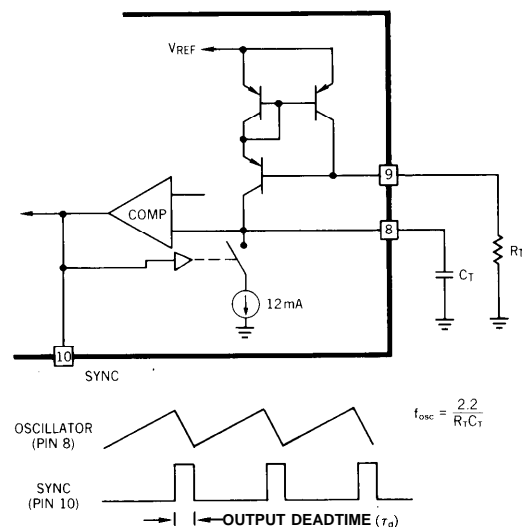


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

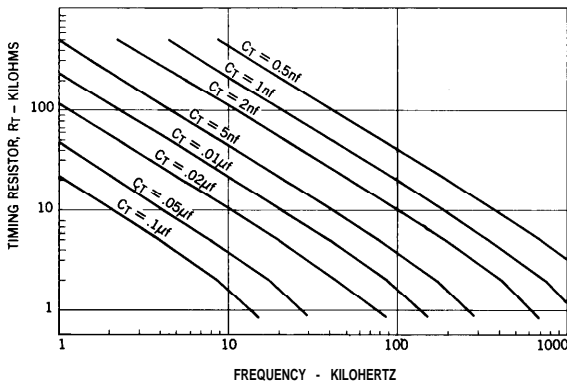


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau_d = 145 C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)} \right] \quad (2)$$

For large values of R_T :

$$\tau_d = 145 C_T \quad (3)$$

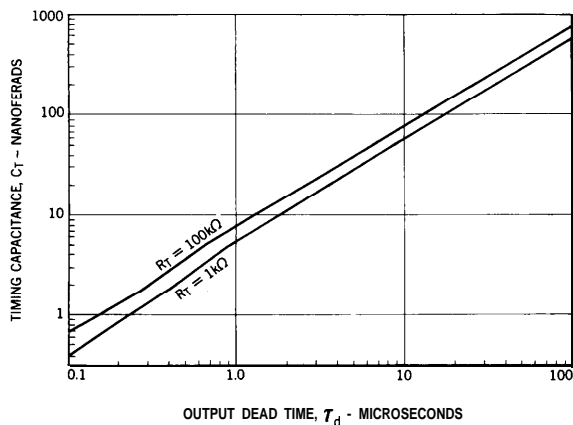


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

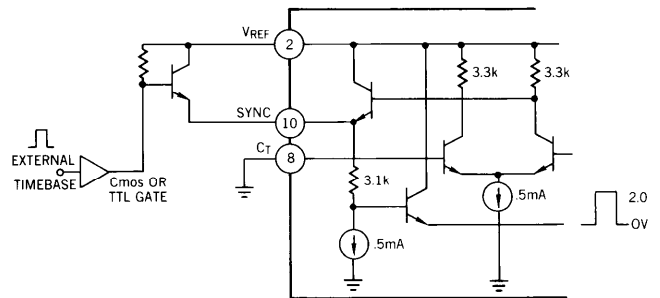


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2 , to set a pre-determined voltage at pin 1.

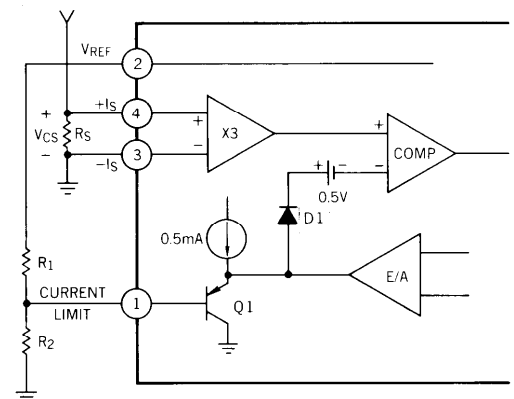


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q₁, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q₁ and the forward drop of diode D₁ very nearly cancel, the negative input of the comparator will be clamped at the value V_{PIN 1} - 0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{R_2 (V_{REF}) - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R₁ also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R₂ as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

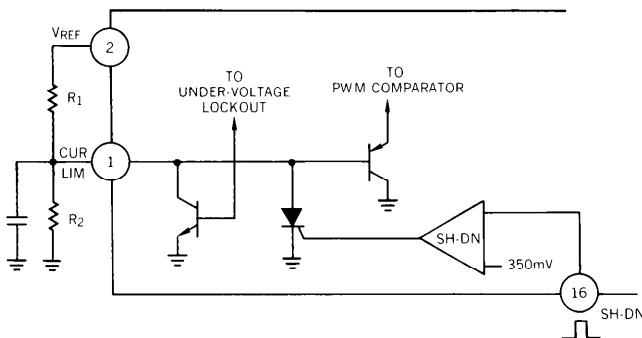


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q₁ requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R₁ is chosen greater than 5kΩ, Q₁ will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R₁ is chosen less than 2.5kΩ, Q₁ will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

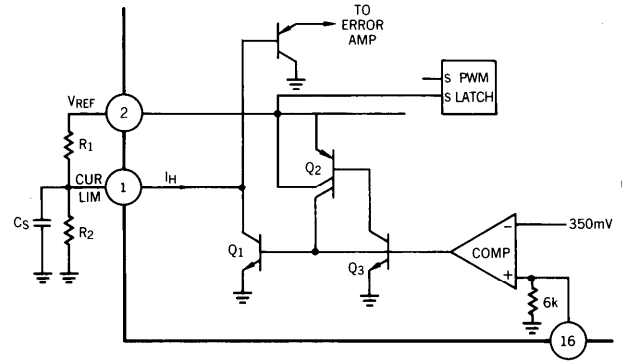


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R₃ and R₄ is exceeded. This level should be greater than the peak current limit value determined by R₁ and R₂ (see equation 5). Sometimes called a “hiccup mode”, this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

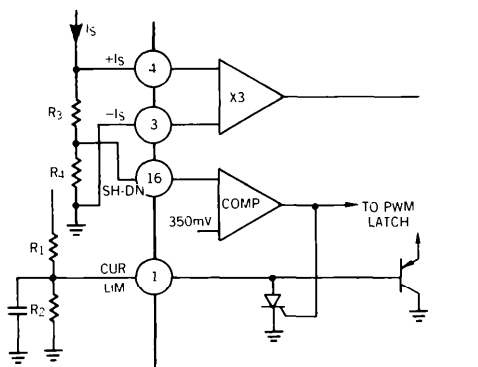


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN - SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads - such as the gates of power FETS - are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz - a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency⁽⁵⁾. Therefore, a pole-zero combination has been

placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation⁽⁴⁻⁶⁾. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation - important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

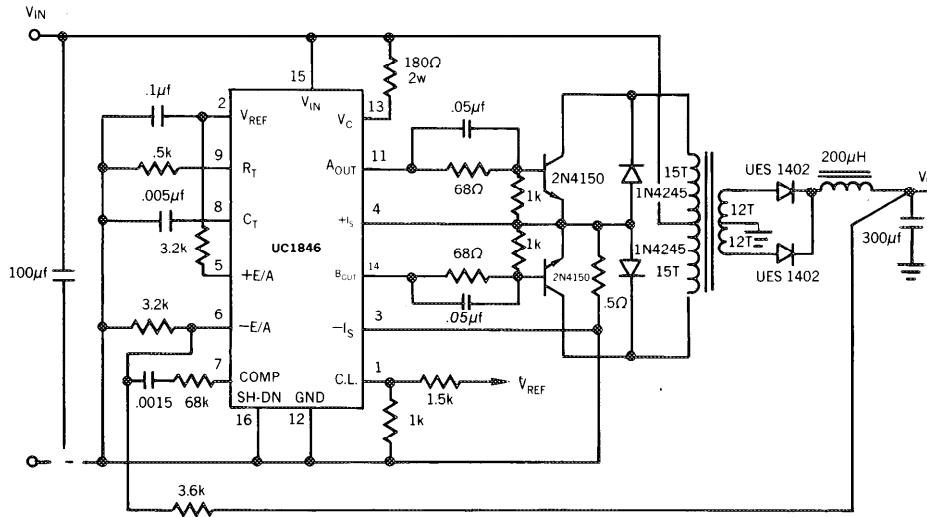
It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF} , -E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response - 40mV as compared to 70mV for the UC1525A.

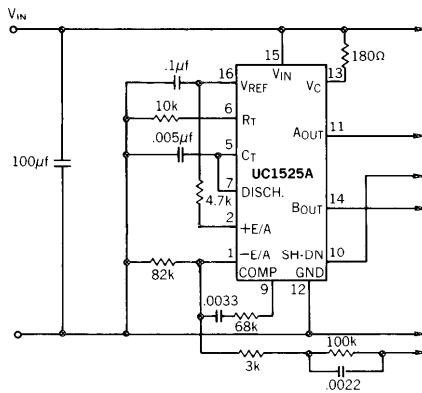
Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A - with identical output

transistors - shows phase B driving the core close to saturation with 50% more current than phase A.

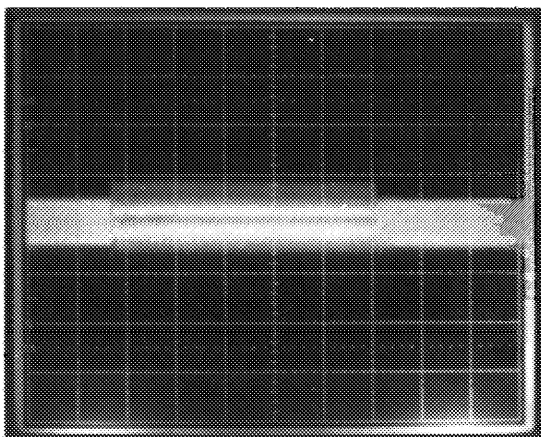


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR

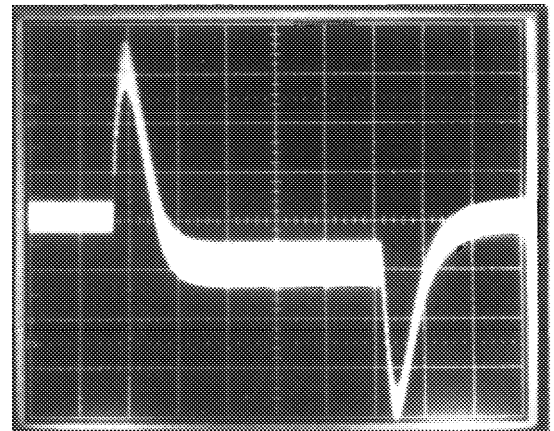


(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A)



(B)

t = 2ms/DIV
 OUTPUT RESPONSE
 50mV/DIV

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS

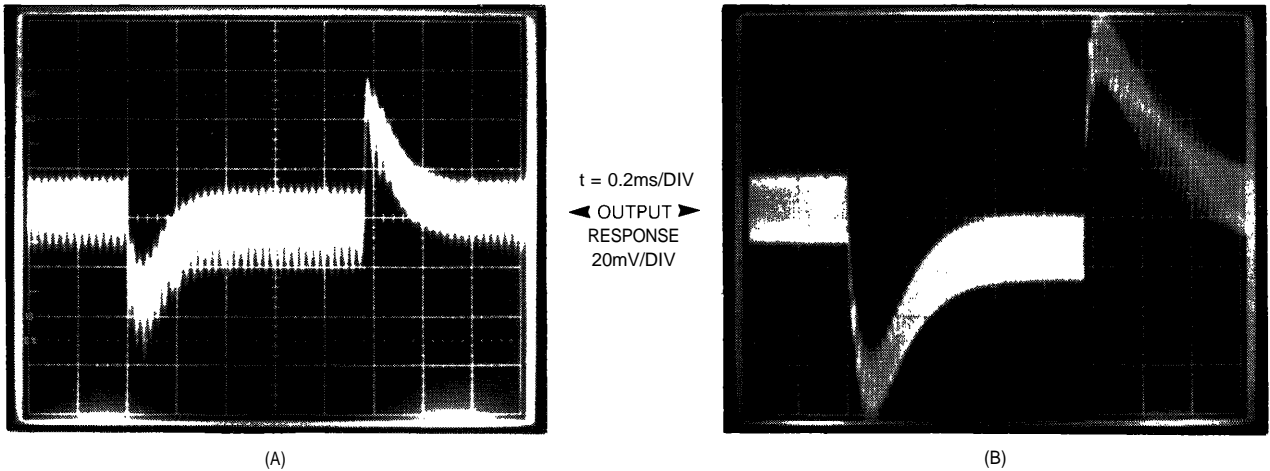


FIGURE 15. RESPONSE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

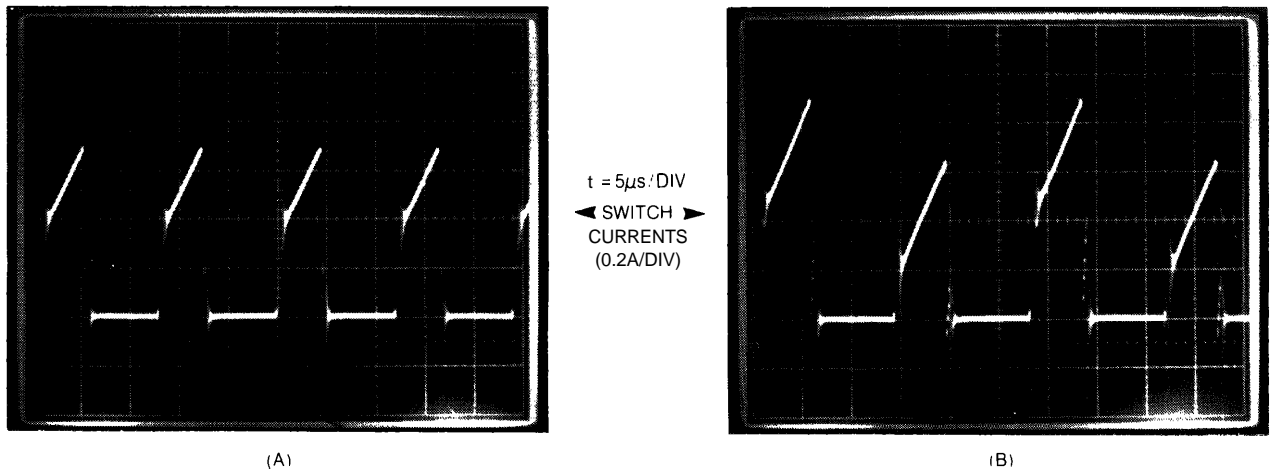


FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular

design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.